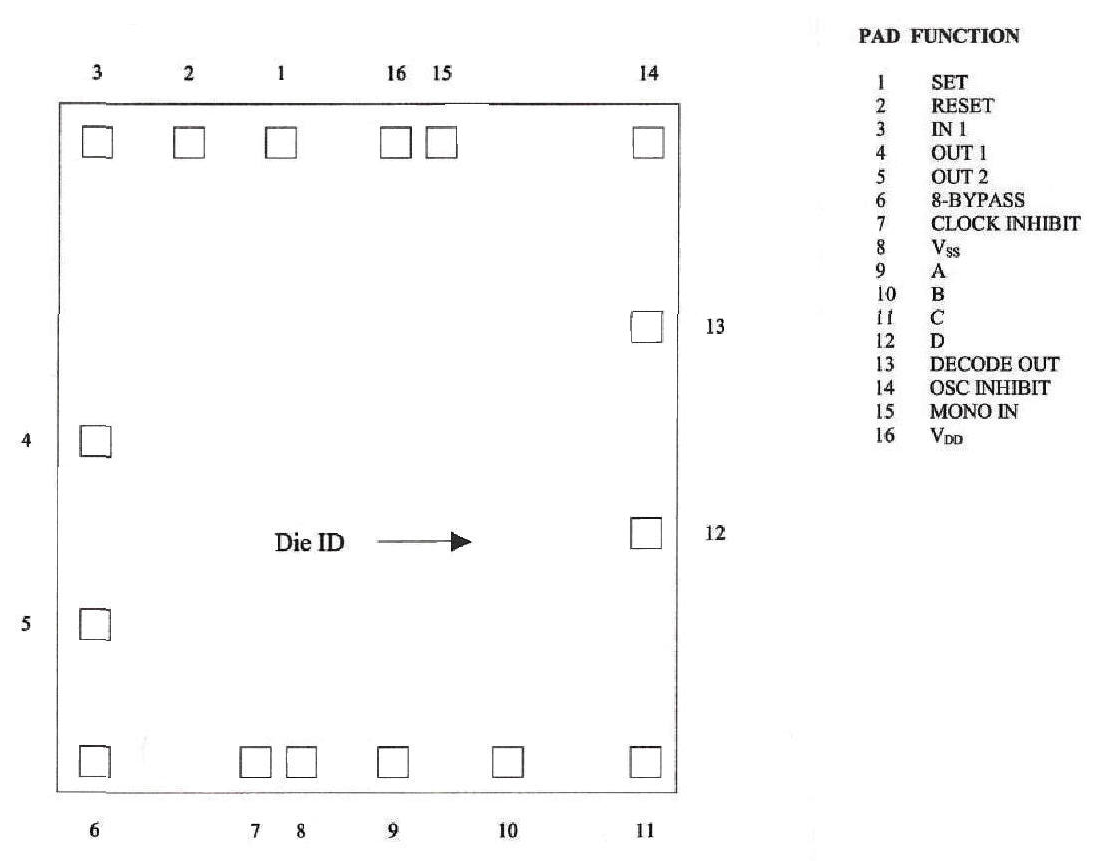
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .095” X .112” DATE: 10/4/21**

**MFG: TIH THICKNESS .025” P/N: CD4536B**

**DG 10.1.2**

#### Rev B, 7/19/02